

This Page Is Inserted by IFW Operations  
and is not a part of the Official Record

## **BEST AVAILABLE IMAGES**

Defective images within this document are accurate representations of the original documents submitted by the applicant.

Defects in the images may include (but are not limited to):

- BLACK BORDERS
- TEXT CUT OFF AT TOP, BOTTOM OR SIDES
- FADED TEXT
- ILLEGIBLE TEXT
- SKEWED/SLANTED IMAGES
- COLORED PHOTOS
- BLACK OR VERY BLACK AND WHITE DARK PHOTOS
- GRAY SCALE DOCUMENTS

**IMAGES ARE BEST AVAILABLE COPY.**

**As rescanning documents *will not* correct images,  
please do not report the images to the  
Image Problem Mailbox.**

**What is claimed is:**

1. A process for forming an electrically conductive metallic interconnect in an via in a dielectric which comprises:
  - providing a dielectric layer in a substrate wherein the substrate comprises electrically conductive lines,
  - forming a trench or via in the dielectric layer and exposing electrically conductive line in the substrate;
  - depositing a first liner layer on the walls and bottom of the trench or via;
  - removing residual contamination from the bottom of the trench or via;
  - depositing a second liner layer on the walls and bottom of the trench or via;
  - depositing a seed layer in the trench or via and
  - filling the trench or via with electrically conductive material.
2. The process of claim 1 wherein the dielectric layer comprises a low-k dielectric having a dielectric constant of less than 3.9.
3. The process of claim 1 wherein the electrically conductive lines comprises copper, aluminum or alloy thereof.
4. The process of claim 1 wherein the electrically conductive lines comprise copper or alloy thereof.
5. The process of claim 1 wherein the first liner layer comprises at least one member selected from the group consisting of comprises n Ta, W, Ti, nitrides and combinations thereof.
6. The process of claim 1 wherein the first liner layer comprises Ta.

7. The process of claim 1 wherein the residual contamination is removed by etching.
8. The process of claim 7 wherein the etching comprises an argon etching.
9. The process of claim 1 wherein the second liner layer comprises at least one member selected from the group consisting of Ta, W, Ti, nitrides thereof and combinations thereof.
10. The process of claim 5 wherein the second liner layer comprises at least one member selected from the group consisting of Ta, W, Ti, nitrides thereof and combinations thereof.
11. The process of claim 1 wherein the second liner layer comprises Ta.
12. The process of claim 6 wherein the second liner layer comprises Ta.
13. The process of claim 1 wherein the seed layer comprises copper.
14. The process of claim 1 wherein the conductive material for filling the trench or via comprises copper.
15. The process of claim 1 which further comprises depositing an adhesion liner layer prior to depositing the first liner layer.
16. The process of claim 15 wherein residual contamination is removed from the bottom of the trench or via prior to depositing the first liner layer.
17. The process of claim 15 wherein the adhesion liner layer comprises a nitride of Ta, W or Ti.
18. The process of claim 16 wherein the adhesion liner comprises TaN.
19. The process of claim 17 wherein the first liner layer comprises at least one member selected from the group consisting of comprises n Ta, W, Ti, nitrides and combinations thereof.

20. The process of claim 19 wherein the second liner layer comprises at least one member selected from the group consisting of Ta, W, Ti, nitrides thereof and combinations thereof.
21. The process of claim 18 wherein the first liner layer comprises Ta.
22. The process of claim 22 wherein the second liner layer comprises Ta.
23. The electrically conductive metallic interconnect obtained by the process of claim 1.
24. The electrically conductive metallic interconnect obtained by the process of claim 16.
25. An electrically conductive metallic interconnect in a via or trench in a via or trench in a dielectric which comprises  
a dielectric layer on a substrate;  
an electrically conductive line in the substrate;  
a via or trench in the dielectric layer;  
liner located on the walls and bottom of the  
trench wherein the liner in the bottom of the trench or via comprises at least one member selected from the group consisting of Ta, W and Ti and which directly contacts the electrically conductive line; and  
electrically conductive material above the liner and filling the trench.
26. The interconnect of claim 25 wherein the liner on the walls of the trench differs from that on the bottom.
27. The interconnect of claim 26 wherein the liner on the walls comprises at least one nitride of a member selected from the group consisting of Ta, W and Ti, and the liner at the bottom comprises at least one member selected from the group consisting of Ta, W and Ti.
28. The interconnect of claim 26 wherein the liner on the walls comprises TaN and the liner in the bottom comprises Ta.

29. The interconnect of claim 28 wherein the electrically conductive material comprises copper.
30. The interconnect of claim 27 wherein the electrically conductive material comprises copper.